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10/650,794	08/29/2003	Ting-Yuan Cheng	TOP 319	7446
7590 10/05/2006		EXAMINER		
RABIN & BERDO, P.C.			ODOM, CURTIS B	
Suite 500 1101 14th Street	t, N.W.	•	ART UNIT	PAPER NUMBER
Washington, DC 20005		•	2611	
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Please find below and/or attached an Office communication concerning this application or proceeding.

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	Application No.	Applicant(s)				
	10/650,794	CHENG, TING-YU	AN			
Office Action Summary	Examiner	Art Unit				
	Curtis B. Odom	2611				
The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply						
A SHORTENED STATUTORY PERIOD FOR REPLY WHICHEVER IS LONGER, FROM THE MAILING DA - Extensions of time may be available under the provisions of 37 CFR 1.13 after SIX (6) MONTHS from the mailing date of this communication. - If NO period for reply is specified above, the maximum statutory period w - Failure to reply within the set or extended period for reply will, by statute, Any reply received by the Office later than three months after the mailing earned patent term adjustment. See 37 CFR 1.704(b).	ATE OF THIS COMMUNICATION 36(a). In no event, however, may a reply be tim vill apply and will expire SIX (6) MONTHS from cause the application to become ABANDONE	I. the mailing date of this co (35 U.S.C. § 133).				
Status						
1)⊠ Responsive to communication(s) filed on 29 Au	ugust 2003.					
	action is non-final.					
3) Since this application is in condition for allowar	· <u> </u>					
Disposition of Claims						
4) Claim(s) 1-10 is/are pending in the application. 4a) Of the above claim(s) is/are withdraw 5) Claim(s) is/are allowed. 6) Claim(s) 1-10 is/are rejected. 7) Claim(s) is/are objected to. 8) Claim(s) are subject to restriction and/or	vn from consideration.		,			
Application Papers						
9) The specification is objected to by the Examiner.						
10)⊠ The drawing(s) filed on <u>8/29/2003</u> is/are: a) accepted or b) objected to by the Examiner. Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).						
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d). 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.						
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Priority under 35 U.S.C. § 119 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a) All b) Some * c) None of: 1. Certified copies of the priority documents have been received. 2. Certified copies of the priority documents have been received in Application No. 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)). * See the attached detailed Office action for a list of the certified copies not received.						
Attachment(s)	•					
1) Notice of References Cited (PTO-892) 2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date	4) Interview Summary Paper No(s)/Mail Da 5) Notice of Informal P 6) Other:	ate				

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

- (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
- 2. Claims 1 and 7 are rejected under 35 U.S.C. 102(b) as being anticipated by Bergmans (U. S. Patent No. 5, 426, 671).

Regarding claim 1, Bergmans discloses a method of signal path tracking for symbol timing recovery in a receiver as shown in Fig. 1, block 6, comprising the steps of:

providing current sampling values for a received signals using samplers in Fig. 1, elements 16 and 20 (see column 8, lines 22-29) to generate current symbols according to sampling instants which represent the timing scheme (see column 7, lines 22-29);

detecting optimal (expected) sample values of the current symbols for sampling the received signal by providing samples to decision circuits (Fig. 1, blocks 26 and 30) to create expected sample values represented by the decisions as described in column 9, lines 3-8 and 14-23);

computing an expected timing error using a phase detector (see Fig. 1, block 28) from the current sampling values and the expected values by correlating the values (see column 8, lines 30-34 and column 9, lines 3-13); and

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adjusting the sampling instants representing a timing scheme using a voltage controlled oscillator (see Fig. 1, block 18, column 8, lines 35-39) to generate a future sampling point by adjusting sampling instants (see column 7, lines 11-16) for a subsequent symbol according to the expected timing error, thereby recovering symbol timing of the receiver by adjusting the sampling instants to minimize the timing error signal (see Abstract).

Regarding claim 7, Bergmans discloses a system of signal path tracking for symbol timing recovery in a receiver comprising:

a symbol sampler as shown in Fig. 1, elements 16 and 20 (see column 8, lines 22-29), sampling a received signal at current sampling instant according to a sampling instants representing a timing scheme (see column 7, lines 22-29);

a decision device (Fig. 1, blocks 26 and 30) representing a peak detector, detecting optimal (expected) sample values represented by the decisions as described in column 9, lines 3-8 and 14-23) for sampling the received signal;

a phase error detector (Fig. 1, block 28), computing an expected timing error (see column 8, lines 30-34 and column 9, lines 3-13) using correlation from the expected sample values detected by the decision circuit and the current sampling values of the symbol sampler; and

a voltage controlled oscillator (see Fig. 1, block 18, column 8, lines 35-39) representing a path tracker, computing a future sampling point by adjusting sampling instants (see column 7, lines 11-16) for a subsequent symbol according to the expected timing error, thereby recovering symbol timing of the receiver by adjusting the sampling instants to minimize the timing error signal (see Abstract).

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Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

- (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 4. Claims 2 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bergmans (U. S. Patent No. 5, 426, 671) as applied to claims 1 and 7, in view of Betts et al. (U. S. Patent No. 6, 853, 695).

Regarding claims 2 and 8, Bergmans discloses the method/apparatus includes a phase detector (Fig. 1, block 28) representing a comparator for comparing (by using correlation) the current sampling values of the symbol sampler and the expected sample values detected by the decision circuit (see column 8, lines 30-34 and column 9, lines 3-13) to obtain timing differences represented by a timing error signal and a loop (low-pass) filter (Fig. 1, block 22) for filtering the timing error received from the phase detector to obtain an average moving error (see column 8, lines 34-35). Bergmans does not disclose an integrator for integrating the average moving error from the loop filter to obtain an expected error.

However, Betts et al. also discloses a method/apparatus for symbol timing recovery (see Fig. 1B), wherein a generated timing phase error is integrated (averaged) by a leaky integrator (see Fig 1B, column 4, lines 60-64), wherein the integration is a moving integration (average) in that it includes the previous timing phase error in the integration (see column 5, lines 32-40). Betts et al. further discloses the output of the integrator is then scaled by a multiplier (element

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53) and fed to an ideal integrator to generate a value which is used to help control a voltage controlled oscillator (VCXO) (see column 5, lines 45-55), wherein the VCXO generates a symbol timing similar to that of Bergmans (see column 6, lines 64-65). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to integrate an average timing error signal in Bergmans as disclosed by Betts et al. to generate a frequency offset value (Δf) obtained from integrating the average error signal (see Betts et al., column 5, lines 45-60) which can be used to help control the voltage-controlled oscillator to generate a symbol timing.

5. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bergmans (U. S. Patent No. 5, 426, 671) as applied to claim 1, in view of Zierhofer. (U. S. Patent No. 6, 128, 103).

Regarding claim 3, Bergmans discloses low-pass filtering the timing error signal comprises convolution and accumulation of timing differences.

However, Zierhofer discloses a low-pass filter which convolves a digital sequence by multiplying and accumulating the digital sequence with the impulse response of the filter.

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the low-pass filtering of Bergmans with the low-pass filtering of Zierhofer since Zierhofer states the low-pass filter can be operated at extremely high modulation frequency with a simple impulse response which requires only a few binary counters with variable increments (see column 3 lines 56-60).

6. Claims 4 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bergmans (U. S. Patent No. 5, 426, 671) as applied to claims 1 and 7, and in further view of Rahnema (U. S. Patent No. 5, 870, 443).

Regarding claims 4 and 9, Bergmans does not disclose the expected (optimal) points for sampling the received signal correspond with samplings of a maximum signal strength in each symbol duration.

However, Rahnema discloses a squared-pulse waveform includes a relatively strong fundamental harmonic at the symbol rate and the maximum points (Fig. 1, point 48) lie in the middle or each bit (see column 3, lines 49-52). Rahnema further discloses the optimal sampling point (Fig. 1, point 48) of the signal corresponds to the maximum signal amplitude point on the waveform (see column 3, lines 63-67), wherein this point is the maximum signal amplitude point of a square wave pulse shape as shown in Fig. 3.

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify timing recovery of Bergmans to include expected (optimal) sampling points which correspond to maximum signal amplitude points as disclosed by Rahnema since Rahnema states that in order to compute the optimum timing phase in a receiver sampling points must correspond to the maximum points on the received waveform (see column 3, lines 58-67).

7. Claims 5 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bergmans (U. S. Patent No. 5, 426, 671) as applied to claims 1 and 7, and in further view of Steckler et al. (U. S. Patent No. 4, 636, 836).

Regarding claims 5 and 10, Bergmans discloses the phase error detector (Fig. 1, block 28) computes a timing error signal for every a_{2i} and a_{2i-1} transmitted symbols as disclosed in (column 7, lines 34-37 and column 8, lines 23-35). Bergmans does not disclose the current sampling values and the expected values for computing the expected error are averages of the two symbols.

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However, Steckler discloses a phase error detector which averages input samples to generate a phase error signal used to lock a clock signal of a timing processor (see column 4, lines 39-43). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to average the inputs to the phase error detector in Bergmans as disclosed by Steckeler et al. since Steckler et al. discloses averaging the input achieves a more accurate phase lock (see column 6, lines 19-22).

8. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bergmans (U. S. Patent No. 5, 426, 671) as applied to claim 1, in view of Kovacs et al. (U. S. Patent No. 5, 646, 968).

Regarding claim 6, Bergmans does not specifically disclose the timing scheme for sampling the received signal is adjusted to continue alignment of a sampling clock transition with an optimal sampling point computed by the expected error of a preceding symbol.

However, Kovacs et al. also discloses timing adjustment for a sampling circuit which compares digital representations of sample points to desired sampling point levels (see column 4, lines 21-31) to generate an error signal which is used to control the timing (phase) of the clock frequency (transitions) of the sampler by use of a voltage-controlled oscillator (see column 4, liens 31-33). Kovacs et al. further discloses the oscillator can output a clock signal which is based on the comparison of the first sample with the desired sample points (column 5, lines 3-14). This continues alignment of the sampling clock by adjusting the sample frequency for subsequent sample points based on the error of the preceding first sampling point (see column 3, lines 53-59). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the method of Bergmans to adjust the sampling clock based on

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expected error of a preceding sample (symbol) as disclosed by Kovacs et al. since Kovacs et al. states proper sampling is necessary for subsequent accurate decoding and processing of a data signal (see column 3, lines 65-67).

Conclusion

- 9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Beherns (U. S. Patent No. 5, 572, 558) discloses adjusting the timing of a sampling clock based on the comparison of sampled values with expected sampled values. Belotserkovsky et al. (U. S. Patent No. 6, 628, 735) disclose adjusting the timing of a sampling clock based detected peak values of the sampled signal.
- 10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Curtis B. Odom whose telephone number is 571-272-3046. The examiner can normally be reached on Monday- Friday, 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on 571-272-2988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Curtis Odom

September 21, 2006